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NPL National Physical Laboratory

Scalable, Monolithic Ion Traps Microfabricated using Planar Silica-on-Silicon Technology

Motivation

Microtraps allow faster shuttling and higher gatespeeds than larger traps. They also lend themselves to integration to many trapping regions [1].

Microtraps have been fabricated from gold coated alumina [2, 3] and gallium arsenide [4]. We propose a trap design based on silica-on-silicon.

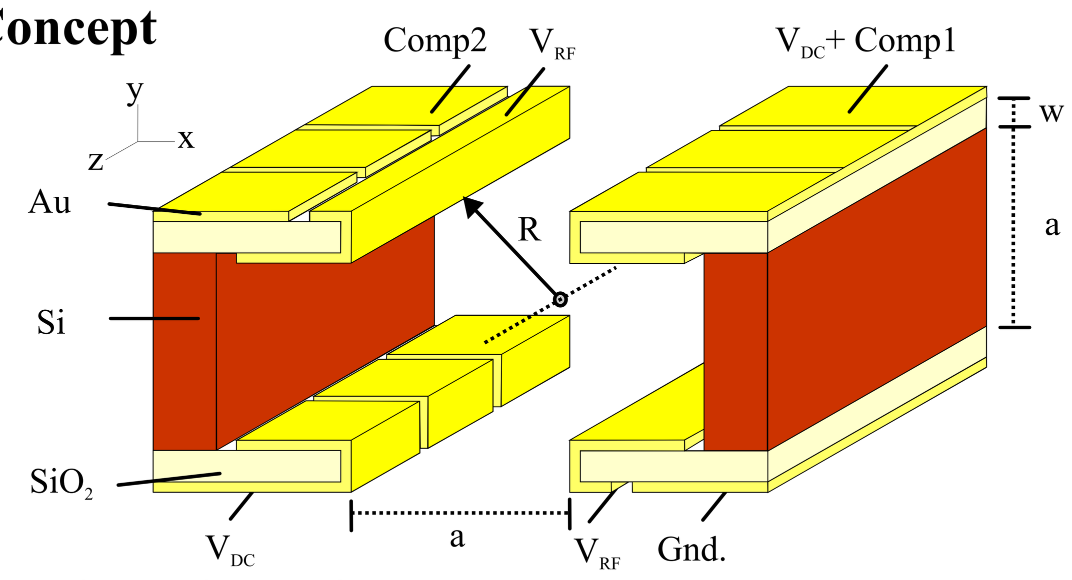
Advantages of Silica-on-silicon traps

- Uses established technology,
- Scalable to many segments,
- Integrable with photonics hardware - eg optical fibres,
- Monolithic - no post-processing assembly of structure,
- Unit aspect ratio - 3D trap from planar processing.
  gives high efficiency => deep potential.

[1] D. Kielpinski *et al*. Nature **417**, 709 (2002)
[2] M.A. Rowe et al, Quant. Inf. Comp. 2, 257 (2002).
[3] W.K. Hensinger et al, Appl. Phys. Lett. 88, 034101 (2006).
[4] D. Stick et al. Nature Physics 2, 36 (2006).

Fabrication

Concept



Physical dimensions

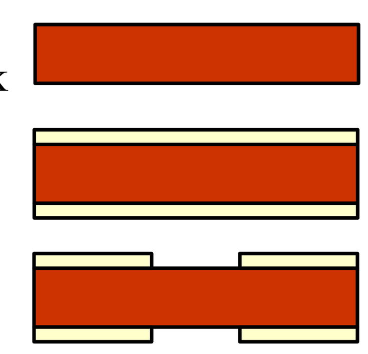
Si Thickness	100 – 500 m
SiO_2 Thickness	20 m
Au Thickness	5 m
Au Surface roughness	10 nm RMS
Undercut	100 – 300 m
Si Resistivity	10^{-4} m

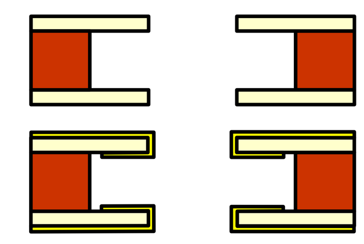
Process

Silicon wafer, 500 100 m thick

Grow thermal oxide up to 20 m thick

Plasma etch to remove SiO_2



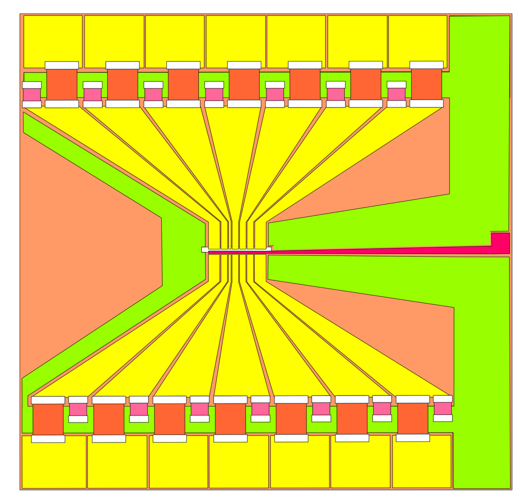


Wet etch to remove Si

Pattern Au electrodes

Process also allows for 3 layer structures (flip-chip bonding) and fibre integration (V-grooves)

Chip layout

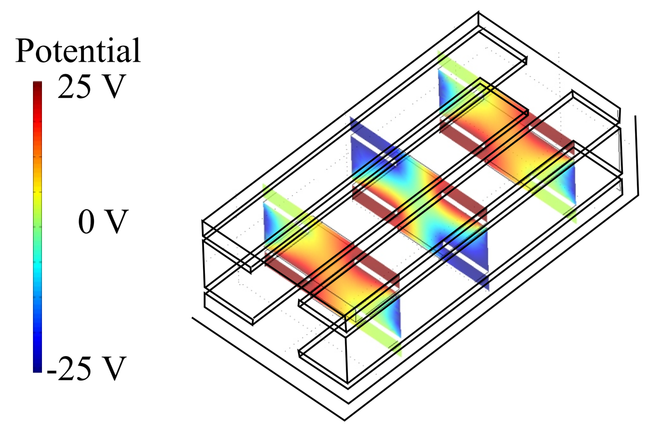


DC and compensation electrodes
RF electrode at one end
Ground electrodes either side of RF
Bare Silica away from trapping region for better radiative heat removal
SMD Resistors
SMD Capacitors

The same pattern (reflected) is on the underside

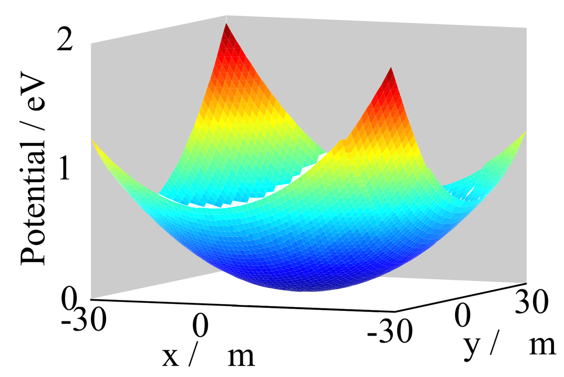
Modelling

Finite element modelling of trap in 2D and 3D to calculate static potentials due to RF and DC electrodes.



Calculate [5] resultant pseudo-potential for $^{88}Sr^+$ using MATLAB.

$$\underbrace{\frac{e}{4M\Omega_T^2}\left|\nabla V_0(x,y,z)\right|^2}_{RF} + \underbrace{V_1(x,y,z)}_{DC}$$



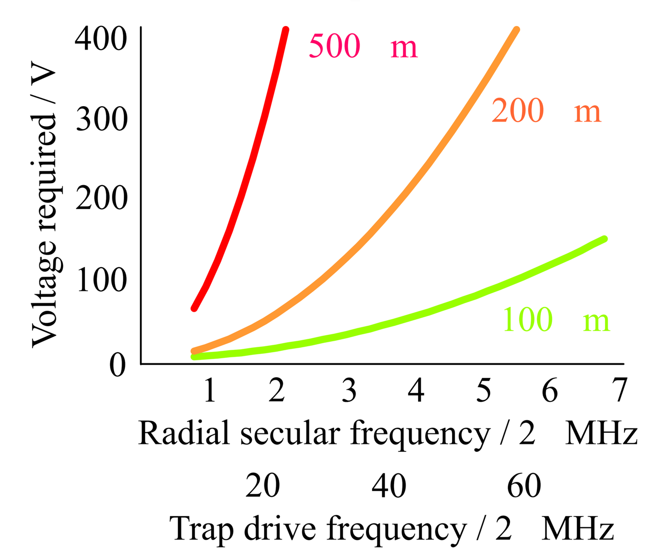
Calculate conditions for stable trap operation in XY plane, assuming $^{88}Sr^+$.

$$q = \frac{2eV_0}{M\Omega_T^2 R^2}$$

$$\Omega_T = \frac{2\sqrt{2}\,\omega_r}{q}$$

$$\omega_r = \sqrt{\frac{eV_0 q}{4MR^2}}$$

V_{RF} required as a function of frequency for q=0.4



Calculate the axial frequency, and perturbation of the radial frequencies due to the end voltage.

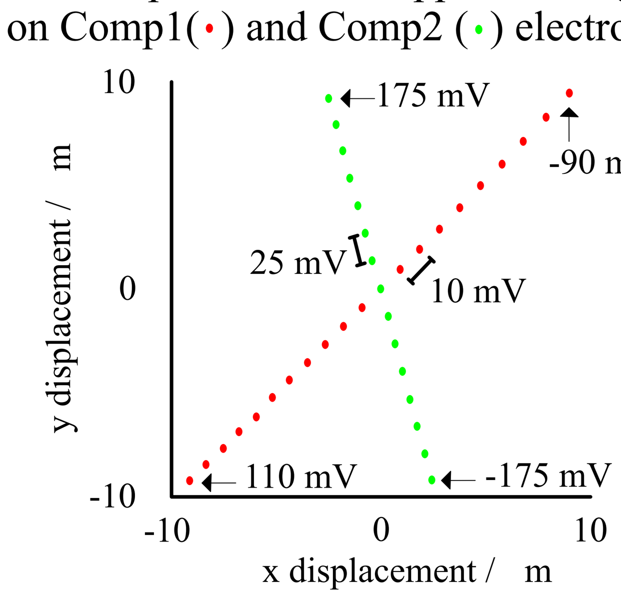
$$\omega_z = \sqrt{\frac{2eV_{DC}}{Mb_{eff}}}$$

[5] M.J. Madsen *et al*. Appl. Phys. B. **78**, 639 (2004)

Typical operating parameters for $^{88}Sr^+$

Parameter					Unit
a	500	200	100	20	m
w	15	15	15	15	m
V_{RF}	350	160	40	10	V
V_{DC}	8	7	2	1	V
RF Freq., $\Omega_T/2$	20	33	33	33	MHz
$\omega_{r1}/2$	2.0	3.4	3.3	10.0	MHz
$\omega_{r2}/2$	1.6	2.8	2.9	6.7	MHz
$\omega_z/2$	1.0	2.5	2.6	5.2	MHz

Ion displacement for applied voltages on Comp1(•) and Comp2 (•) electrodes.

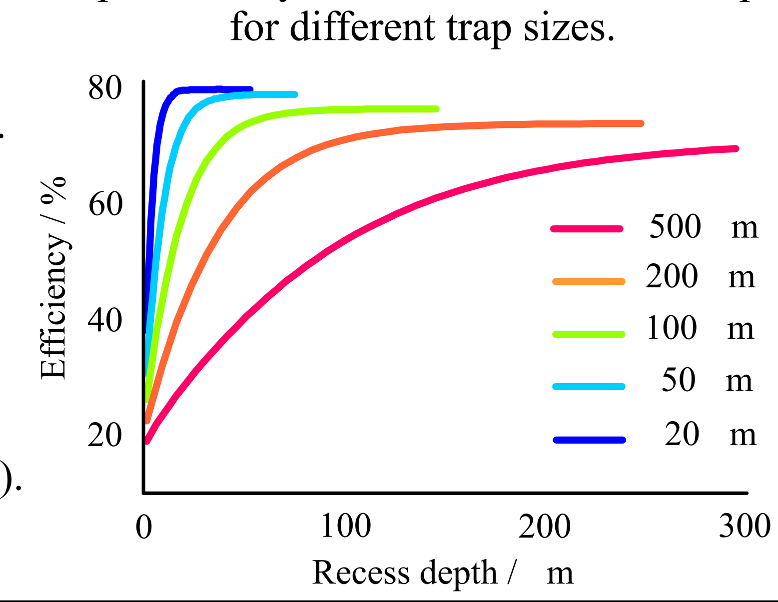


Practicalities

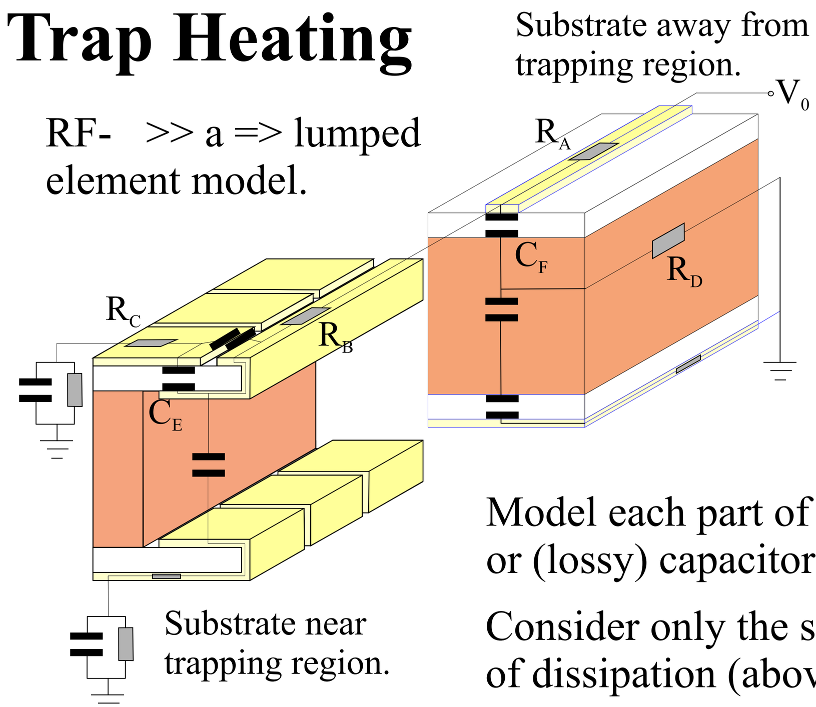
Micromotion compensation (figure left)
Compensation voltage added to DC electrodes (Comp1). and to segmented pattern behind RF (Comp2)
Allows micromotion compensation in 2D.

Efficiency (figure right)
Proximity of silicon substrate effects trap efficiency.
Negligible if recess is deeper than ~1.5 a.
Smaller traps have higher efficiency (see figure far right).

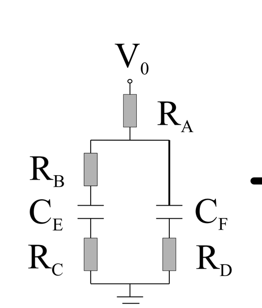
Trap efficiency as a function of recess depth for different trap sizes.



Trap Heating

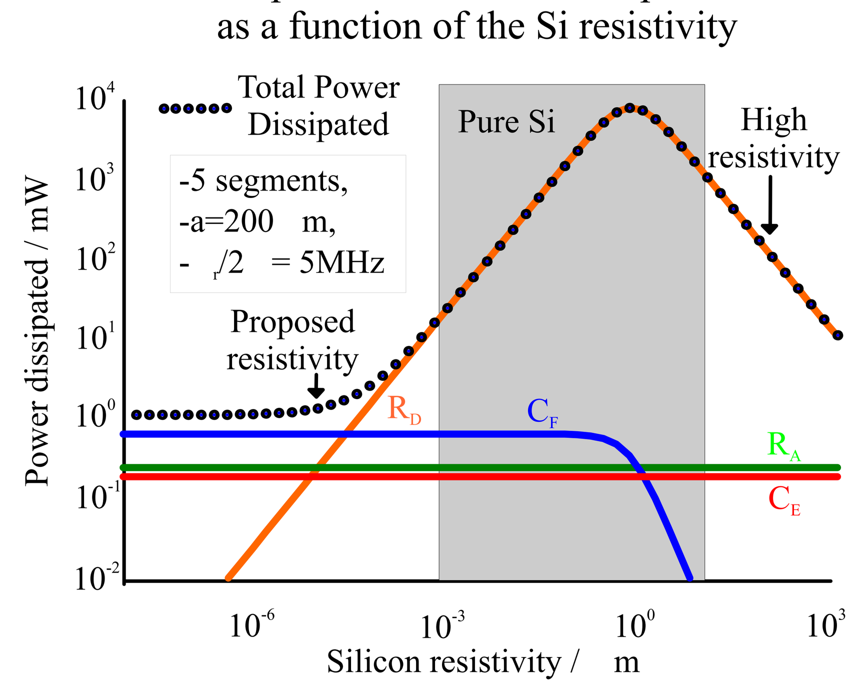


RF- >> a => lumped element model.



Model each part of trap as resistors or (lossy) capacitors (left).
Consider only the significant sources of dissipation (above).

Dissipation in different components as a function of the Si resistivity



Temperature Increase

Si is good thermal conductor
- no localised heating.

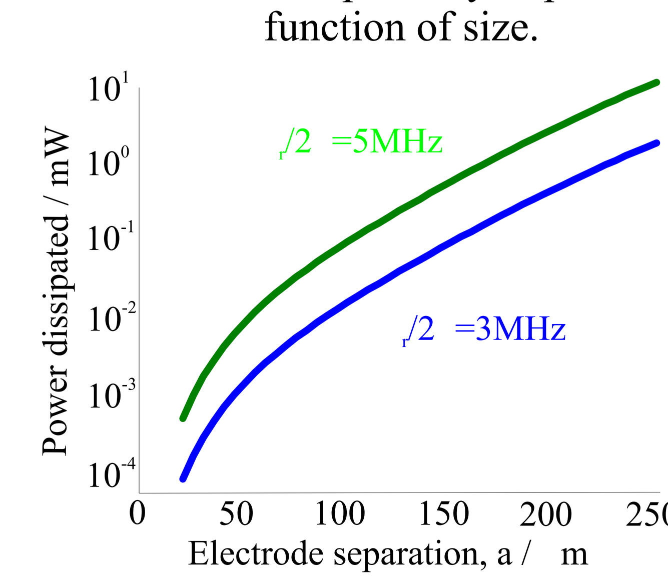
Worst case:
- pure radiative heat removal,
- Au coated chip (low emissivity),

for 15 x 15 mm chip, 1 mW => T=12°C.
Improves if some silica left bare.

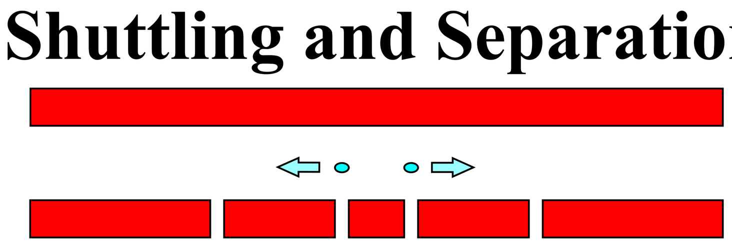
Size dependence

Smaller traps require lower RF voltages for the same motional frequency.
Power dissipated decreases with trap size.

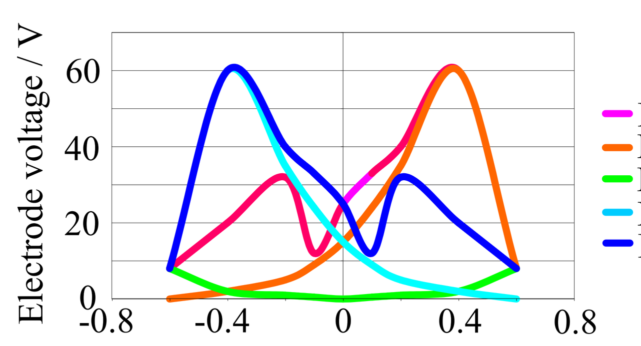
Power dissipated by traps as a function of size.



Shuttling and Separation



Have modelled DC voltage requirements for shuttling and separation of ions using SIMION and FEMLAB.



Progress

Trap fabrication underway for 500 m, 250 m & 150 m thick wafers.
First Fabrication run expects to yield:

Thickness	Wafer yield	# different designs	# chips per design
500 m	3	3	6
250 m	3	4	6
150 m	1	2	2

Will use SMD capacitors and resisters for on-chip low pass filtering.
Have 2nd set of filters outside vacuum chamber.

Chip to be mounted on macor holder, and wire bonded to 2nd level packaging.

Conclusion

- We have designed a linear RF ion trap, microfabricated from gold coated silica-on-silicon. The electrodes are formed by patterened gold on silica cantilevers.
- Design can be fabricated using standard processing techniques, and is integrable with photonics technologies such as filters switching and optical fibres.
- Requires no assembly of electrodes after processing, and is scalable to many segment geometries.
- Fabrication underway for trap sizes to 100 m ion-electrode separation (i.e. 150 m wafer). Smaller traps may be feasible.

This work is supported by NPL's strategic research programme, and by EU contracts IST-2001-38875-QGATES and IST 2005-15714-SCALA